multiLane

DATASHEET

Innovation for the next generation

ML8008FX-SIA

8-Lane TDR | TDA
4-Lane 112GBd High Speed I/O

Time Domain Reflectometry | S-Parameter Measurement | Eye Pattern Measurement | BER Measurement |

Summary

In today's extremely competitive and fast-paced industry, time is the most expensive form of currency. Every second saved is a step ahead of the competition. This is what MultiLane is all about; with our high performance, automated and throughput optimized solutions, MultiLane completely redefines the status quo of large-scale production testing.

The state-of-the-art solutions we provide are fully automated and engineered for the sole purpose of providing our customers with accurate and reliable measurements while also saving them valuable time.

MultiLane's ML8008FX-SIA joined our large and diverse collection of successful products as a signal integrity analyzer allowing tests, NRZ & PAM4 eye diagram measurements, as well as medium impedance characterization and S-parameter evaluation.

ML8008FX-SIA

Introduction

The ML8008FX-SIA is a state-of-the-art combination of a TDR, Digital Sampling Oscilloscope and BERT. The DSO performs accurate eye- diagram analysis at 70 GHz to characterize the quality of transmitters and receivers, implementing a statistical under-sampling technique with comprehensive software libraries for eye measurements, jitter analysis and processing of NRZ/PAM4 data. The true-differential TDR can determine the impedance profile and reflection loss on 8 channels simultaneously. It is designed and suited both for characterization as well as manufacturing. The BERT that can be configured at 224G, 112G and 56G PAM4 and 25G NRZ and their derivative dynamic rates. It is compliant with the IEEE 802.3ck C2M, OIF CEI 112G VSR, MR and LR. The transmitters support all standard test patterns mandated by the specs such as PRBS13Q, SSPRQ, PRBS31Q, etc. Tx can also be programed to output a user-defined pattern. Additionally, the transmitter and receiver equalization is up to 40dB to overcome signal integrity impairments due to channel losses or reflections.

7 ps Rise Time TDR and Time Domain Analyzer

Key Features

TDR/TDT features

- High Resolution TDR/TDT Single-Ended and Differential measurements
- 7 ps Rise Time, Time Domain Reflectometry / Transmission optimized for high-speed tests and measurements.
- Impedance Profile Measurement
- Determination of the magnitude and polarity of any back reflected signal
- 8 ports per module expandable up to 32+
- 8x70 GHz analog bandwidth in TDT mode
- Modular & Scalable
- Optimized for HV Manufacturing
- Extremely fast throughput (sub-second)
- Simple and Fast KGU calibration
- Time/Frequency Domain Measurements

S-parameters

- Return loss
- Insertion loss
- Crosstalk

Electrical specifications

Parameter	Specifications
Data format support	NRZ and PAM-4
Intrinsic jitter	200 fs rms
Electrical amplitude	< 600 mV SE and < 1200 mV Diff
Rise/Fall Time	7 ps (including cables + conn.)
Vertical resolution	14 bits
SFDR	46dB @ 10GHz
ENOB	11.7 bits
Noise Floor	1.2 mV_{rms} (1. 5 mV_{rms} max)
Electrical channel bandwidth	70 GHz
Electrical channel connectors	(2X) 1X4 ML SMPS
Clock input bandwidth (PLL mode)	0.1 - 4.5 Gsps
Sampling frequency	50 - 80 MHz
Data Input	AC coupled
Pattern Capture	SSPRQ & Up to PRBS-16
Normal Operating Temperature	0 - 70 °C
Instrument Automatic Shutoff	70 °C (manual reboot is needed for turn on when temperature < 65 °C)
Power rating	31W

Supported Measurements

Coding	Measurement
PAM-4	TDECQ
	SNDR
	RLM
	OMA_{outer}
	Eye Height by BER
	Eye Width by BER
NRZ	Top & Base
	Min & Max
	One & Zero
	Transition Time
	Crossing %
	AOP
	OMA
	Mask Margin
	Peak to Peak
	Eye Amplitude
	Eye Height
	Eye Width
	Jitter
	SNR
	ER
	VEC
	Vrms
	DJ & RJ
	Noise

Use Cases

- High Density Backplane Cables & Connectors
- DAC, AEC, ACC Cables

Number Of Units Needed to Test			
8 Diff Lanes	16 Diff Lanes	32 Diff Lanes	64 Diff Lanes
1	2	4	8

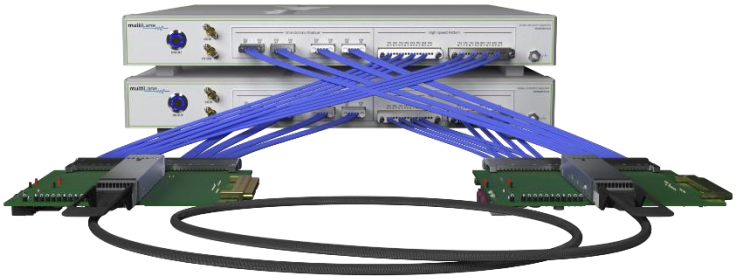

Figure 1 2x ML8008FX-SIA for testing 16 differential pairs DUT

1.6T, 8x 224G High Speed I/O

Key Features

Transmit

- Data Rates: 224G, 112G and 56G PAM4 (+ their dynamic derivatives), 25G NRZ and its derivative.
- Ability to tune the bit rate in steps of 100 kbps and find the RX PLL locking margin
- DFE and CTLE Equalization.
- Independent control of inner eye levels.
- Supports Gray coding.
- 3-tap Pre- and Post-emphasis or 7-tap linear FFE.
- Real hardware FEC. SER and FEC measurements and margin available on channels individually as well as on 800G, 400G, 200G, 100G and 50G.
- Available patterns:
    - PRBS7/9/11/13/15/16/23/31/58
    - PRBS13Q, PRBS31Q
    - SSPRQ
    - Square wave
- Burst and random noise injection.

Receive

- SNR monitoring over time.
- 15-FFE Taps monitor.
- Independent PLL per lane.
- PAM histogram monitor.
- Error-detection on following patterns:
    - PRBS 7/9/11/15/16/23/31
    - PRBS13Q and PRBS31Q
- Automatic pattern detection.
- LOS indicators.
- Up to 40dB Equalization Capabilities.

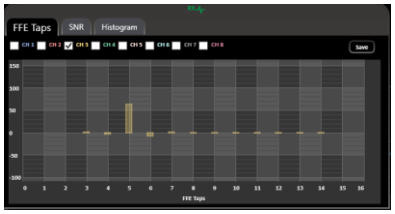

Figure 2 RX FFE Taps

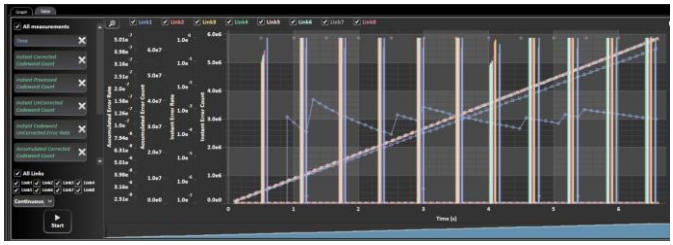

Figure 3 BER Measurements

Electrical specifications

Parameter		Specifications
Bit Rates		224G, 112G and 56G PAM4 and 25G NRZ and their derivative dynamic rates.
TX Amplitude Differential		0 – 800mVpp
Patterns		PRBS 7/9/11/13/15/16/23/31/58/9_4 SQ16, SQ32, LIN, CJT, JP0838, SSPRQ, User Defined
TX Amplitude Adjustment		Steps of 1 mV
Pre-emphasis resolution		1000 steps
Pre- / Post-emphasis		6 dB
Equalizing Filter Spacing		1 UI
Random Jitter RMS [1]		< 350 fs
Rise/ Fall Time (20–80%) [1]		TBD
Coding		Gray coding supported
FEC (up to 800G)		800G/400G/200G/100G/50G
Error Detector input range		50 – 800 mV differential
TX/RX connectors		1x 16 SMPS Connector
Reference clock Output	Reference clock	156.25 MHz
	Monitor clock	Rate division /2 to /32
Diff. Input Return Loss		Better than 10 dB
Eye monitor resolution		8 bits horizontal across 2 UI / 9 bits vertical
Clock Input Range		Up to 4.4 GHz
Clock Input Amplitude		800 – 1600 mV
Input Impedance		50 Ω
Ambient Temperature		0 – 75 °C

[1] With appropriate pre and post emphasis settings and 50 GHz scope. Trigger from adjacent data channel rate/8

Ordering Information

Option	Description
ML8008FX-SIA	224G Signal Integrity Analyzer
3YW	Total 3-year warranty
CAL	Single calibration
3YWC	Total 3-year warranty with 3 annual calibrations

Recommended Accessories

TBD			

Please contact us at sales@multilaneinc.com.

This equipment contains ESD sensitive components and may become damaged when contacted with an electrostatic charge. To prevent equipment damage, please use proper grounding techniques.